

FIG. 1

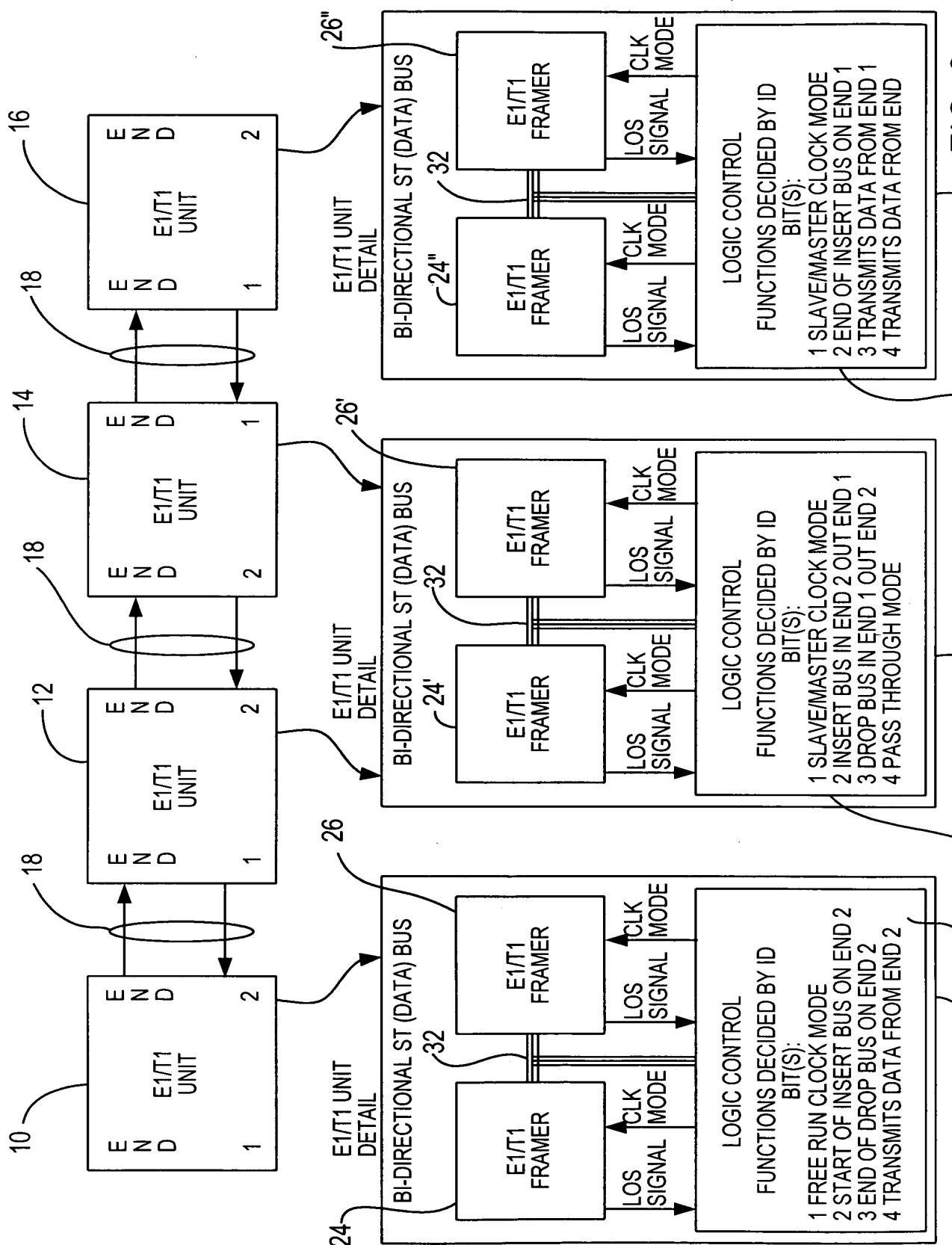


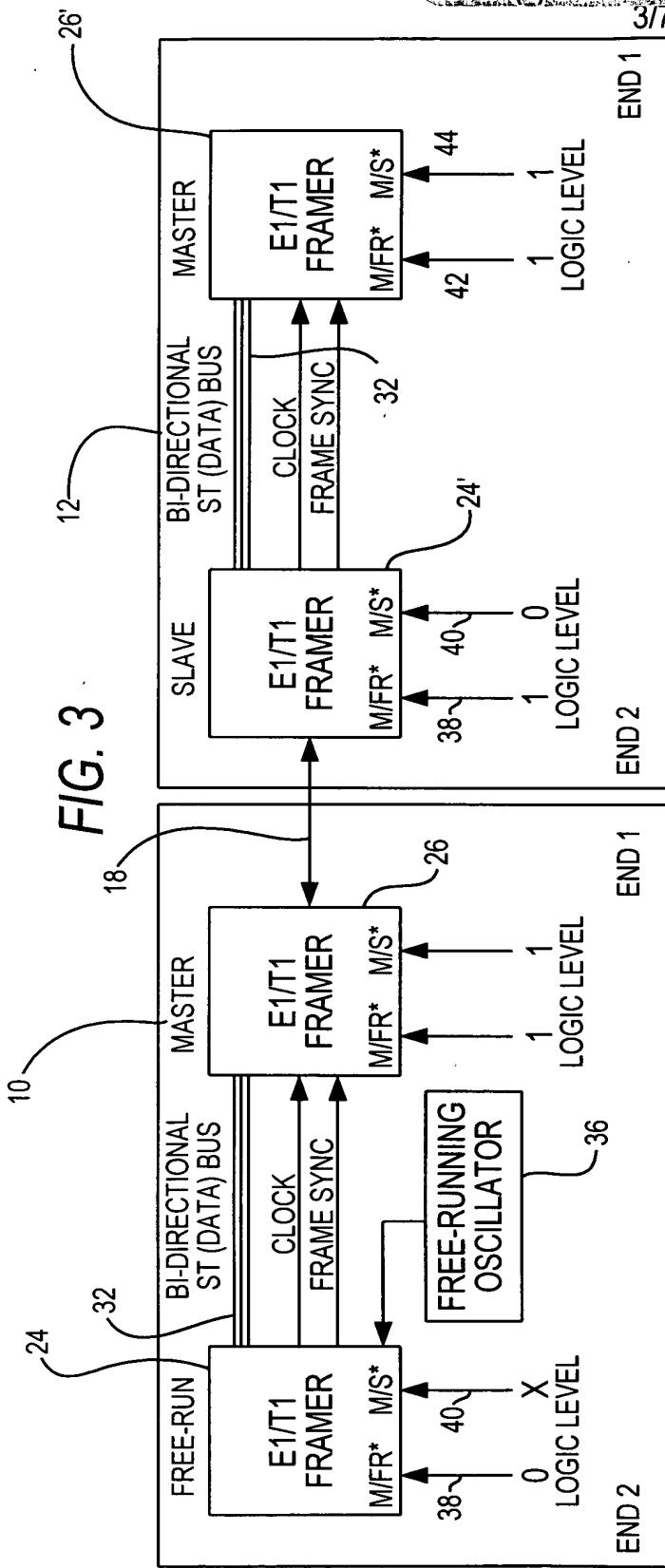
FIG. 2

34

12

34

10



**FRAMER CHIP MODE CONTROL TABLE**

MODE	MASTER	FREE RUN	SLAVE	FREE RUN	LOGIC LEVEL
	0 1 0 1	X 0 X 1			

**INPUT SIGNAL PIN NAME**

MASTER-SLAVE/NOT FREE RUN
MASTER-NOTSLAVE

**FIG. 3A**

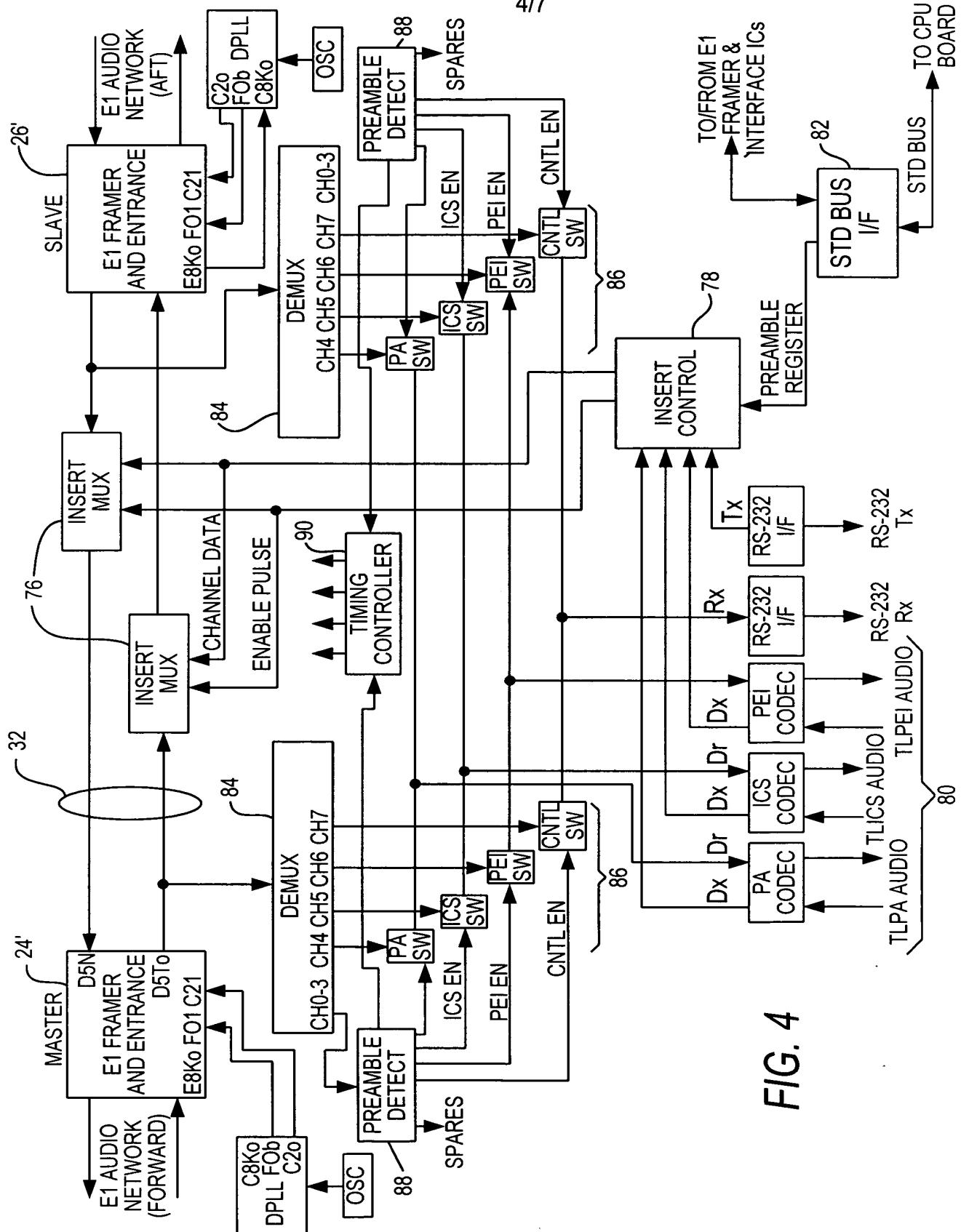


FIG. 4

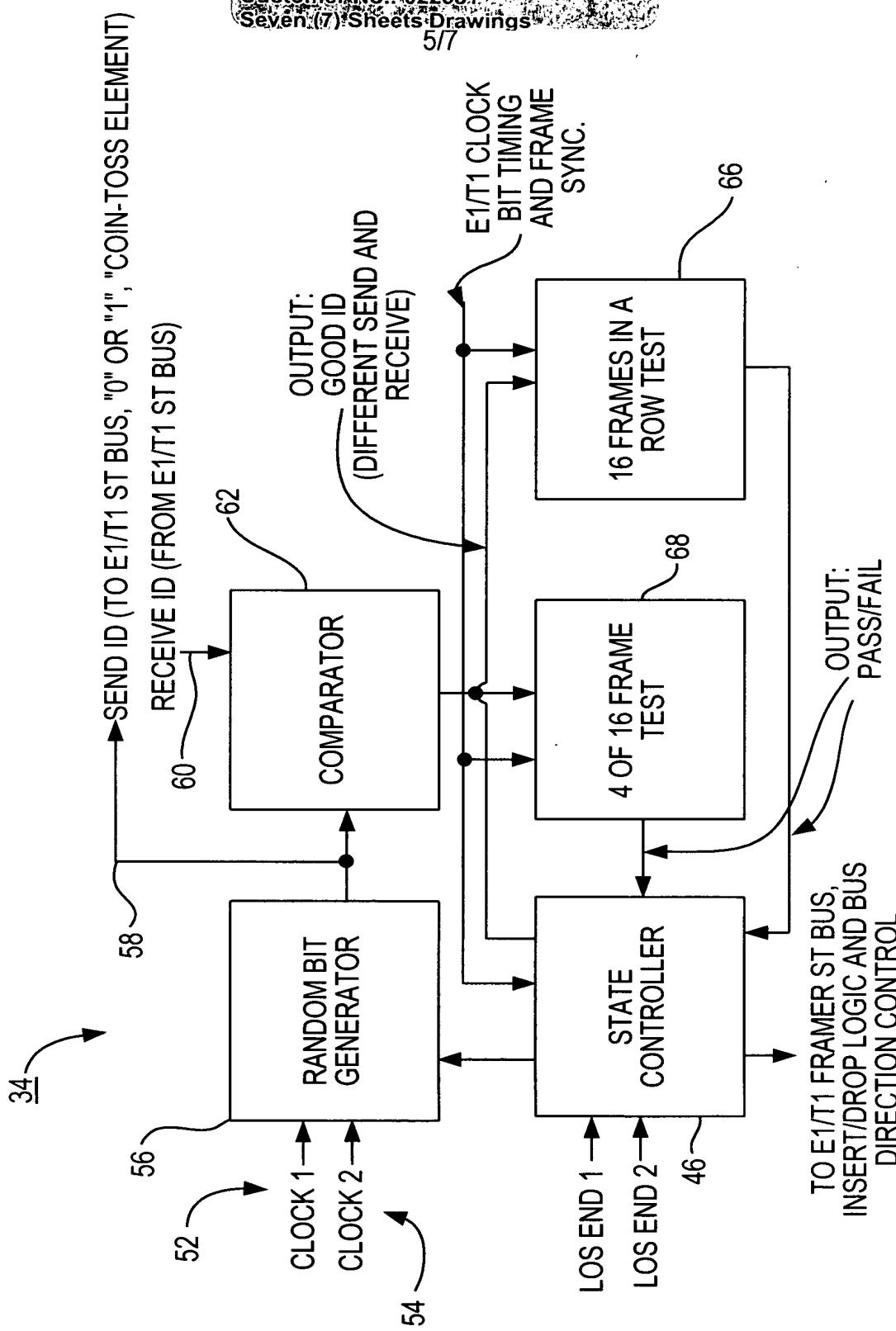


FIG. 5

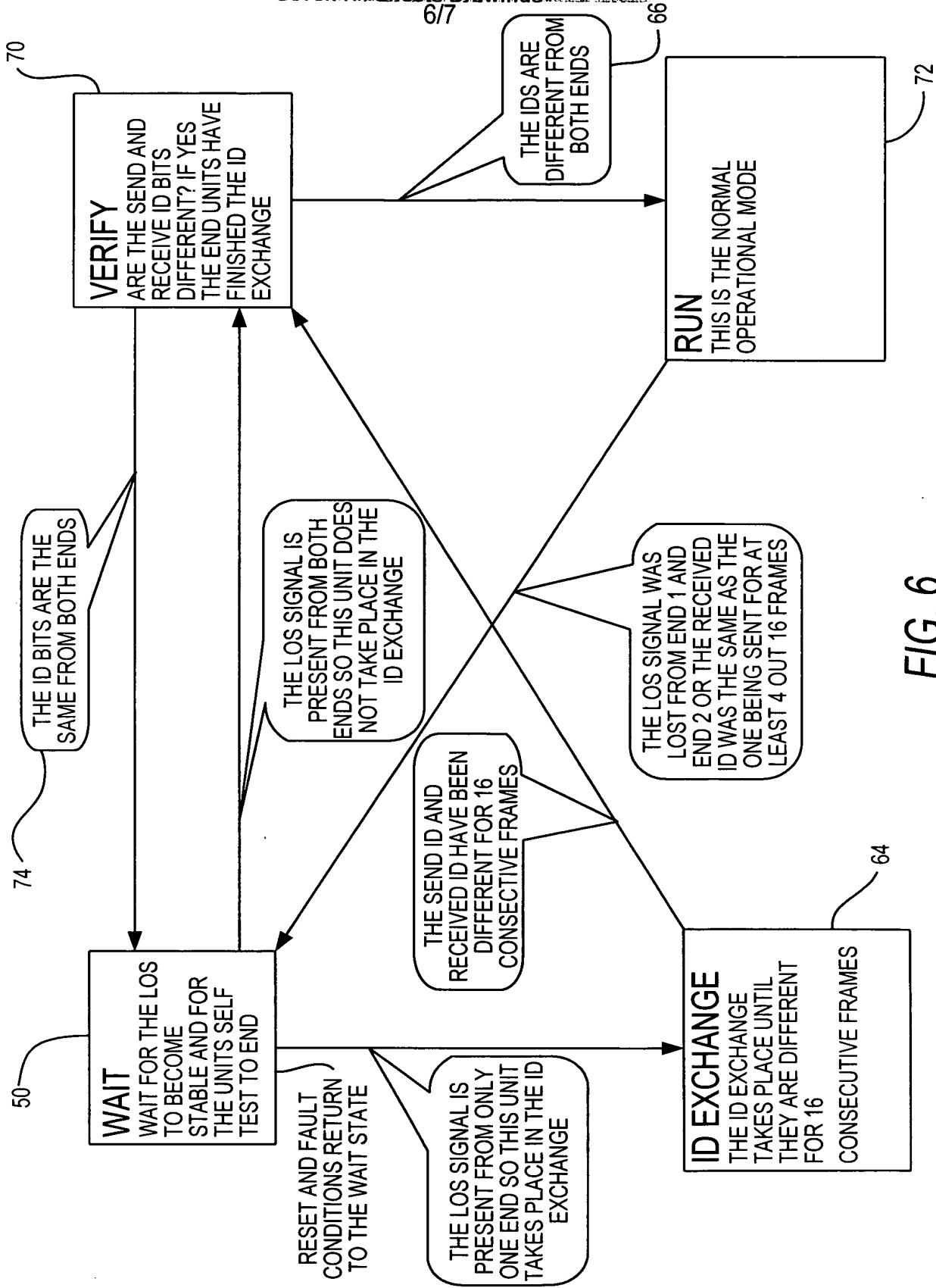


FIG. 6

